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SEMICONDUCTOR WAFER PROCESSING DEVICE

Inventors: Makoto Yoshida
Fujitsu Denki K.K.
1-1 Nitta Tanabe,
Kawasaki-ku
Kawasaki-shi, Kanagawa-ken

Applicant: Fujitsu Electric Co., Ltd.
1-1 Nitta Tanabe,
Kawasaki-ku
Kawasaki-shi,
Kanagawa-ken

Agent: Isao Yamaguchi, patent attorney

[There are no amendments to this patent.]

Claim

[The present invention concerns] a semiconductor wafer processing device for a processing system that processes the surface of semiconductor wafers one at a time, and is a semiconductor wafer processing device characterized in that, along with being equipped with a heating means that preheats the semiconductor wafer before the surface processing, a cooling means that cools the semiconductor wafer after the surface processing, and a wafer-raising and lowering mechanism that, along with having the function of holding the semiconductor wafer and advancing and retracting, raising and lowering, and rotating horizontally, takes the semiconductor wafer before the surface processing from outside said vacuum vessel to within said vessel, and a transport mechanism that delivers the semiconductor wafer to a wafer stage inside the above-mentioned processor reaction chamber after preheating by means of the above-mentioned heating means, is installed in a closed condition without mutual partitions being provided between each other within a single vacuum vessel that is transported by a vacuum gate valve to a processor reaction chamber wherein surface processing is executed on a semiconductor wafer, with wafer raising and lowering mechanisms on which the semiconductor wafer is carried and which move the semiconductor wafer in the vertical and horizontal directions beneath said heating means and cooling means, respectively, and said vacuum vessel is formed so that it is able to be connected in an airtight manner to a cassette chamber, which accommodates a cassette in which the semiconductor wafers

are carried, at the heating means on the side opposite the transport mechanism.

Detailed explanation of the invention

Industrial application field

This invention relates to an [illegible] processing type of semiconductor wafer processing device which conducts surface processing such as thin-film formation and etching by means of plasma CVD and the like one wafer at a time on semiconductor wafers (hereinafter, simply called wafer).

Prior art

A design example of the semiconductor wafer processing device used until now is shown in Figure 6. In the Figure, (1) is the processor reaction chamber, (2) is a plasma-generating chamber wherein a magnetron (4) used as a microwave generator is connected by waveguide (3) and the excitation coil (5) is installed on the circumference of the chamber; (6) is a load-and-lock chamber that is connected by the vacuum gate valve (7) to the processor reaction chamber (1); (8) is a vacuum gate valve that gates the load-and-lock chamber (6) and the atmosphere; (9, 10) are vacuum exhaust systems that are connected to the processor reaction chamber (1) and the load-and-lock chamber (6), respectively; (11) is a wafer-support mechanism provided with, for example, an electrostatic chuck (12), which is inside the processor reaction chamber (1) facing opposite the plasma-

generating chamber (2); and (13) is a cassette in which a plurality of semiconductor wafers (14) are accommodated.

With this type of design, the processor reaction chamber (1) and the plasma-generating chamber (2) are evacuated, the microwaves that are generated by the magnetron (4) are transmitted through the waveguide (3) in a condition with the raw material gas carrier gas used for plasma generating corresponding to the purposes supplied from an external source to within the plasma-generating chamber (2), and by means of applying a magnetic field by flowing current through the excitation coil (5), an ECR plasma is generated within the plasma-generating chamber.

Before this is started, one wafer is sent to inside the processor reaction chamber (1) by means of a transport mechanism present later and accepted and held in the wafer support mechanism (11). In other words, first, N_2 gas is introduced to within the load-and-lock chamber (6) through a conduit that is not illustrated from an external section, and the inside of the chamber is restored to atmospheric pressure. Next, the vacuum gate valve (8) is opened, and after the transport mechanism (15) transports the wafer (14) from the cassette (13) in which the unprocessed wafers are accommodated to inside the single piece handling load-and-lock chamber (6) and rotates, it stands by facing in the direction of the processor reaction chamber (1). Here, the load-and-lock chamber is again held in a vacuum condition by means of the vacuum exhaust system (10), and when the pressure of the load-and-lock chamber (6) reaches a vacuum pressure that is equal to that of the processor reaction chamber (1) the vacuum gate valve (7) is opened, the above-mentioned transport mechanism (15) places the wafer (14) inside the

processor reaction chamber (1), and along with the wafer-support mechanism (11) being delivered inside the chamber, the vacuum gate valve (7) is again closed.

If an ECR plasma is generated as mentioned before while sending a film-forming raw material gas such as, for example, silane gas, inside the processor reaction chamber (1) in this condition, this plasma is forced into the processor reaction chamber (1), the above-mentioned silane gas is activated, and due to the action of the activated [illegible] that was generated by this means, various thin films of different silicon groups are formed by means of the [illegible] of the carrier gas on the surface of the wafer (14).

On the other hand, when the prescribed wafer processing is completed, the wafer (14) is returned to the cassette (13) from the wafer-support mechanism (11) by a routine that is opposite of the above-mentioned insertion operation, and following that, the processing operation for the next wafer is conducted. Also, when the processing is completed for all of the wafers (14) that are accommodated within the cassette (13), after again releasing the vacuum gate valve (8) of the load-and-lock chamber (6), the cassette (13) is taken outside the chamber, the next cassette is inserted in its place, and the wafer processing is conducted by the same type of operations as mentioned above.

Problems to be solved by the invention

However, the unprocessed wafers are exposed to the atmosphere in this type of plasma CVD device, moisture is adhered and other impure gases are adhered, and in the event the processing is conducted in that condition, voids and the like are

generated, the film quality of the film made drops, and the yield and quality of the wafers is deteriorated. The wafer is at a high temperature (about 200°C) immediately after being processed with this type of a plasma CVD device or the like, and also, frequently it is the case that polypropylene is used in the material for the cassette used in the conventional [illegible] device and the like, and there was the problem that if [the wafer] was transferred as is immediately to the cassette, the cassette was deformed. In order to eliminate this problem, the inventors of this invention previously proposed a semiconductor wafer processing device that was equipped with a preheating chamber which housed a heating means such as an integral heater or the like, and a cooling means that accommodated a cooling stage based on water cooling or the like. The semiconductor wafer processing device according to this proposal is one wherein, along with a preheating chamber being connected by a vacuum gate valve (8) to the cassette (13) side of the load-and-lock chamber (6) in Figure 6, a cooling chamber was connected by a vacuum gate valve with the load-and-lock chamber (6) in a direction perpendicular to the face of the paper of Figure 6, but during the preheating of a semiconductor wafer, a wafer for which the surface processing had been completed could not be transported out to inside the cassette (13), the vacuum gate valve had to be opened every time to mutually deliver a wafer between the preheating chamber, the load-and-lock chamber, and the cooling chamber, and because of the lost time required in the opening and closing operations for the vacuum gate valve, in the event this type of device was used on a practical mass production scale, there was a problem generated in the throughput.

The purpose of this invention is to solve these problems and to offer a semiconductor wafer processing device in which film forming with excellent film quality is possible.

Means to solve the problems

In order to solve the above-mentioned problems, in this invention, a semiconductor wafer processing device for an [illegible] processing system that processes the surface of semiconductor wafers one at a time, along with being equipped with a heating means that preheats the semiconductor wafer before the surface processing, a cooling means that cools the semiconductor wafer after the surface processing, and a wafer-raising and lowering mechanism that, along with having the function of holding the semiconductor wafer and advancing and retracting, raising and lowering, and rotating horizontally, take the semiconductor wafer before the surface processing from outside said vacuum vessel to within said vessel, and a transport mechanism delivers the semiconductor wafer after preheating by means of the above-mentioned heating means to a wafer stage inside the above-mentioned processor reaction chamber, is installed in a closed condition without mutual partitions being provided between semiconductor wafer and transport mechanism within a single vacuum vessel that is transported by a vacuum gate valve to a processor reaction chamber wherein surface processing is executed on a semiconductor wafer, and with wafer-raising and lowering mechanisms on which the semiconductor wafer is carried and which move the semiconductor wafer in the vertical and horizontal directions beneath said heating means and cooling means, respectively. Said vacuum vessel is formed so that it is

able to be connected in an airtight manner to a cassette chamber, which accommodates a cassette in which the semiconductor wafers are carried, at the heating means on the side opposite the transport mechanism.

Function

First, in order to facilitate the understanding of the operation, an explanation is given in regard to the operating routine for a semiconductor wafer processing device that is constructed according to the above-mentioned means.

First, the inside of a cassette chamber that is connected by a vacuum gate valve to the atmosphere side of a vacuum chamber that constructs a load-and-lock chamber is returned to atmospheric pressure and installed. After installation, evacuation is conducted. With the load-and-lock chamber and the connected vacuum gate valve in a released condition, a single wafer is taken out from the cassette by means of a transport mechanism within the load-and-lock chamber, is set inside the load-and-lock chamber, and at a heating zone wherein a heating means is arranged, is delivered to a wafer-raising and lowering mechanism that is installed beneath said heating means. During wafer processing, the transport mechanism again removes a single wafer from the cassette chamber and delivers it to the raising and lowering mechanism of the heating zone. Next, the wafer-raising and lowering mechanism moves to the optimum heating position of the heating zone and conducts the heating process. After the process is completed, the wafer-raising and lowering mechanism lowers to the delivery position and delivers the wafer to the above-mentioned transport mechanism. The transport

mechanism to which a wafer has been delivered rotates, and stands by facing the processor reaction chamber, the vacuum gate valve that is connected to the processor reaction chamber is opened, and after the wafer that is standing by is transferred to within the processor reaction chamber, it is delivered to the wafer-support mechanism that is installed within the chamber. Here the transport mechanism returns to inside the load-and-lock chamber and after the vacuum gate valve is closed, the prescribed wafer processing is conducted inside the processor reaction chamber. During wafer processing, the transport mechanism again removes a single wafer from the cassette chamber and delivers it to the wafer-raising and lowering mechanism of the heating zone. Next, the wafer-raising and lowering mechanism is moved to the optimum heating position of the heating zone, the wafer is preheated, and stands by.

When the wafer processing is completed, the processed wafer is moved to the load-and-lock chamber from the processor reaction chamber by a routine that is the opposite of the above-mentioned insertion operation. The above-mentioned transport mechanism delivers it to the wafer-raising and lowering mechanism that is installed beneath the cooling means within the cooling zone that is installed within the load-and-lock chamber; the wafer-raising and lowering mechanism moves to the optimum position of the cooling zone and [the wafer] is cooled. Furthermore, the transport mechanism takes the wafer from the wafer-raising and lowering mechanism of the heating zone, and delivers it to the wafer-support mechanism within the processor reaction chamber in the same manner as mentioned above. Here, the prescribed wafer processing is conducted again, the transport mechanism again takes a single wafer from the cassette chamber, and delivers it

to the wafer-raising and lowering mechanism of the heating zone. Here, the wafer-raising and lowering mechanism moves to the optimum position of the heating zone; the wafer is preheated, and stands by.

After the wafer-raising and lowering mechanism of the heating zone has completed moving to the prescribed position, the transport mechanism takes a wafer from the wafer-raising and lowering mechanism of the cooling zone, passes beneath the wafer-raising and lowering mechanism of the heating zone, and inserts it at the same position as the position from which it was taken from the cassette within the cassette chamber.

In the same manner, the processes are repeated for the designed number of wafers. In this way, according to the device mechanism of this invention, in the wafer transporting process, the cassette chamber, the load-and-lock chamber, and the processor reaction chamber are always maintained at a vacuum and are not opened to the atmosphere side, there is almost no absorption of moisture, insertion of impure gases, or intrusion of debris from external sections, and the inside of the chambers are maintained in a very clean condition.

By this means, even though a wafer is delivered within the processor reaction chamber, there is almost no carrying of foreign substances such as dust from external sections to inside the processor reaction chamber, the moisture on the wafer is removed by means of preheating, and the quality of the thin films that are formed in the wafer can be improved by a wide margin. Also, one can get by with a minimum of opening and closing operations of the vacuum gate valve between each chamber, which becomes the origin of lost time generation in the wafer transporting process, and because the entire chamber is always

under a vacuum condition, the operations of returning to atmospheric pressure and again evacuating become unnecessary, and along with the lost time being eliminated, a sequential process, wherein the wafers on which the cooling process has been completed can be transported out to the cassette during the preheating [of another wafer], becomes possible, the required time for a single series of wafer transport processes are greatly shortened, and an increase in the throughput can be accomplished.

Application examples

Figure 1 is a plan view showing one application example of a semiconductor wafer processing device mechanism of this invention; Figure 2 is a vertical cross-sectional view of the device in Figure 1 through line (A-A), and Figure 3 is a vertical cross-sectional view of the device in Figure 1 along line (A-B). Also, Figures 4 and 5 are cross-sectional views along lines (C-C) and (D-D) in Figures 2 and 3, respectively, and the same components corresponding to Figure 6 have the same keys applied.

First, in Figure 1, the load-and-lock chamber (26) is connectively installed by a vacuum gate valve (7) to the side of the processor reaction chamber (1), and the transport mechanism (15), heating zone (16), and cooling zone (17) are installed within the load-and-lock chamber (26). Also, the cassette chamber (18) is continuously connected to the load-and-lock chamber (26) by vacuum gate valve (19), and is partitioned from the room outside the atmosphere side by means of vacuum gate valve (8). As shown in Figure 2, the feed mechanism (20) which feeds one pitch at each stage of the cassette (13) and the vacuum exhaust system (21) are provided in the above-mentioned cassette chamber (18);

the load-and-lock chamber (26) is equipped with the heating means (22) that is formed as a integral heater and the wafer-raising and lowering mechanism in (23), and as is shown in Figure 3, a cooling stage (24) based on water cooling and a wafer-raising and lowering mechanism (23) are installed inside the load-and-lock chamber (26).

Next, an explanation is given following the routine for the transporting and processing operations for a wafer in the semiconductor wafer processing device comprising the above-mentioned construction.

First, the cassette chamber (18) (Figure 2) is returned to atmospheric pressure, and the cassette (13) is inserted. After insertion, evacuation is conducted by means of the vacuum exhaust system (21). Next, the vacuum gate valve (19) is opened, and the transport mechanism (15) takes a single wafer (14) from the cassette (13) inside the cassette chamber (18), and delivers it to the wafer-raising and lowering mechanism (23). The wafer-raising and lowering mechanism (23) raises the wafer (14) to the optimum position with the heating means (22), makes contact, and here preheating is conducted by means of the heating means (22). After the preheating process is completed, the wafer-raising and lowering mechanism (23) lowers, the wafer (14) is again delivered to the transport mechanism (15), and next, the transport mechanism (15) rotates, faces the processor reaction chamber (1) and stands by, and when the vacuum gate valve (7) is opened, it advances and delivers the wafer (14) to the wafer support mechanism (11) that is installed inside the processor reaction chamber (1), and after retracting, the above-mentioned vacuum gate valve (7) closes. Here, the prescribed wafer processing is conducted.

On the other hand, during wafer processing, the transport mechanism (15) again takes a single wafer (14) by the above-mentioned same routine from the cassette (13), and delivers the wafer to the wafer-raising and lowering mechanism (23) of the above-mentioned preheating zone (16). Here, the wafer-preheating process is conducted. The transport mechanism (15) that has delivered the wafer stands by in a condition facing the processor reaction chamber (1). When the wafer processing is completed, the transport mechanism (15) removes the wafer (14) for which the processing is completed by a routine the opposite of the above-mentioned insertion operation. The wafer (14) that has been transported out is moved to the cooling zone (17) (Figure 1, Figure 3) by means of the above-mentioned transport mechanism (15), and is delivered to the wafer-raising and lowering mechanism (23). Here, the wafer (14) is cooled by means of the cooling stage (24). Also, the transport mechanism (15) that has delivered the wafer (14) to the cooling zone (17) feeds a wafer (14) that has been treated by the heating zone (16) by the above-mentioned same routine to the wafer-support mechanism (11) within the processor reaction chamber (1). Here, the prescribed wafer process is again conducted. Next, the transport mechanism (15) again takes a single wafer (14) by the above-mentioned same routine from the cassette (13), and delivers the wafer to the wafer-raising and lowering mechanism (23) of the above-mentioned preheating zone (16). Here, the preheating is conducted.

Next, the transport mechanism (15) takes the wafer (14) that has been cooled from the wafer-raising and lowering mechanism (23) of the cooling zone (17), and removes it beneath the wafer table of the wafer-raising and lowering mechanism (23) of the

cooling zone (16), and inserts it into the same position of the cassette (13) as the position from which it was removed.

After that, the processing for the prescribed number of components are repeated in the same manner.

Effect of the invention

As was presented above, in this invention, an [illegible] processing type of semiconductor wafer processing device which processes semiconductor wafers one at a time, along with being equipped with a heating means that preheats the semiconductor wafer before the surface processing, a cooling means that cools the semiconductor wafer after the surface processing, and a wafer-raising and lowering mechanism that, along with having the function of holding the semiconductor wafer and advancing and retracting, raising and lowering, and rotating horizontally, takes the semiconductor wafer before the surface processing from outside said vacuum vessel to within said vessel, and a transport mechanism delivers the semiconductor wafer after preheating by means of the above-mentioned heating means to a wafer stage inside the above-mentioned processor reaction chamber, is installed in the closed condition without mutual partitions being provided between transport mechanism and semiconductor wafer, and within a single vacuum vessel that is transported by a vacuum gate valve to a processor reaction chamber wherein surface processing is executed on a semiconductor wafer, and with wafer-raising and lowering mechanisms on which the semiconductor wafer is carried and which move the semiconductor wafer in the vertical and horizontal directions beneath said heating means and cooling means, respectively. Since it is a device wherein the

said vacuum vessel is formed so that it is able to be connected in an airtight manner to a cassette chamber, which accommodates a cassette in which the semiconductor wafers are carried, at the heating means on the side opposite the transport mechanism, in the wafer transporting process, the cassette chamber, load-and-lock chamber and processor reaction chamber are always maintained at a vacuum, there is no release to the atmospheric side, there is almost no moisture adhesion, impure gas adhesion, and intrusion of dust from external sections, and the inside of the chamber is maintained in a high state of cleanliness. By this means, even though the wafer is delivered between [stages] within the processor reaction chamber, the carrying of foreign substances such as dust from external sections to within the processor reaction chamber is almost eliminated. Also, because the surface processing is conducted in a condition wherein the moisture that has adhered to the wafer is removed due to preheating by means of a heating means, the film quality of the thin film that is formed on the wafer is improved, and this film quality becomes possible by means of wafer-raising and lowering mechanisms that are respectively installed beneath a heating means and a cooling means, and a minimum of opening and closing operations of the vacuum gate valves. By means of a sequential processing which transports wafers out of the cassette after the completion of cooling during the preheating of unprocessed wafers, the required time for a series of wafer transporting processes can be shortened by a wide margin compared to prior devices, and the effect of increasing the throughput can be obtained.

Brief description of the figures

Figures 1-5 show the construction of a semiconductor wafer processing device according to one application example of this invention; Figure 1 is a horizontal cross-sectional view of the main section; Figure 2 is a vertical cross-sectional view of the device along line (A-A) in Figure 1; Figure 3 is a vertical cross-sectional view of the device along line (A-B) in Figure 1; Figure 4 is a frontal cross-sectional view along line (C-C) in Figure 2; Figure 5 is a frontal cross-sectional view along line (D-D) in Figure 3; and Figure 6 is a vertical cross-sectional view showing a design example of a semiconductor wafer processing device used until now.

1 Processor reaction chamber
6, 26 Load-and-lock chamber (vacuum vessel)
7, 19 Vacuum gate valve
13 Cassette
14 Semiconductor wafer
15 Transport mechanism
16 Preheating zone
17 Cooling zone
18 Cassette chamber
22 Heating means
23 Wafer raising and lowering mechanism
24 Cooling stage (cooling means)

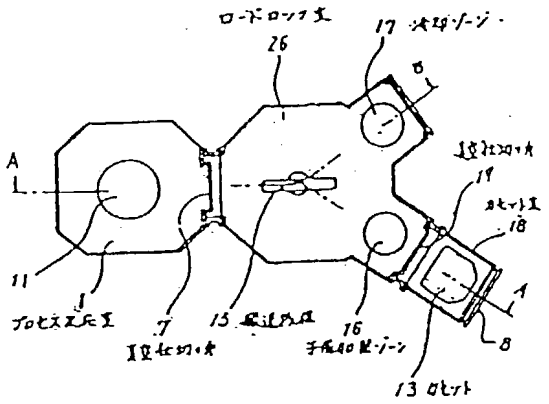

Figure 1

Key: 1 Processor reaction chamber
7, 19 Vacuum gate valve
13 Cassette
15 Transport mechanism
16 Preheating zone
17 Cooling zone
18 Cassette chamber
26 Load-and-lock chamber

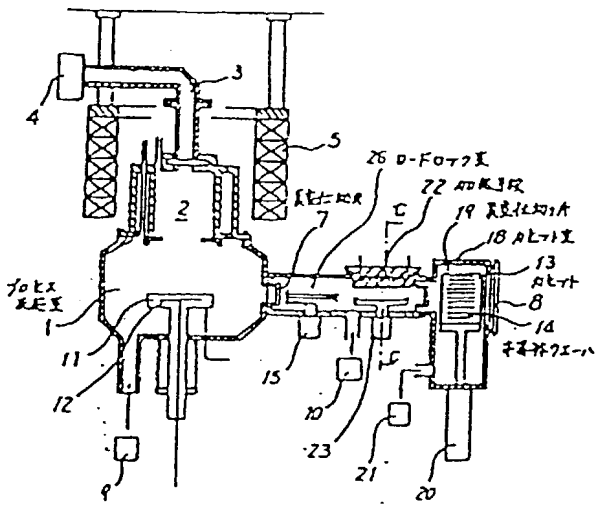

Figure 2

Key: 1 Processor reaction chamber
7, 19 Vacuum gate valve
13 Cassette
14 Semiconductor wafer
18 Cassette chamber
22 Heating means

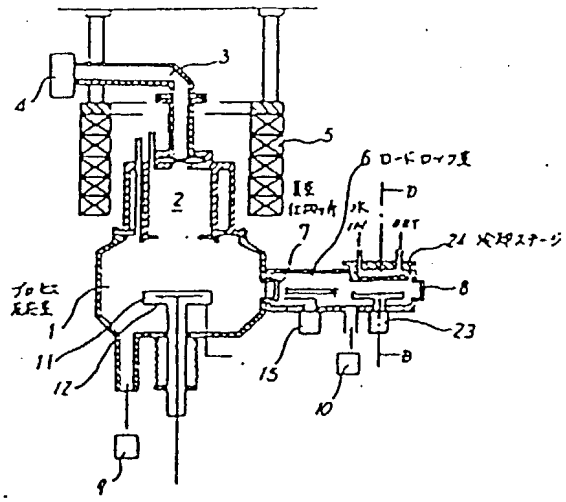

Figure 3

Key: 1 Processor reaction chamber
6 Load-and-lock chamber
7 Vacuum gate valve
24 Cooling stage

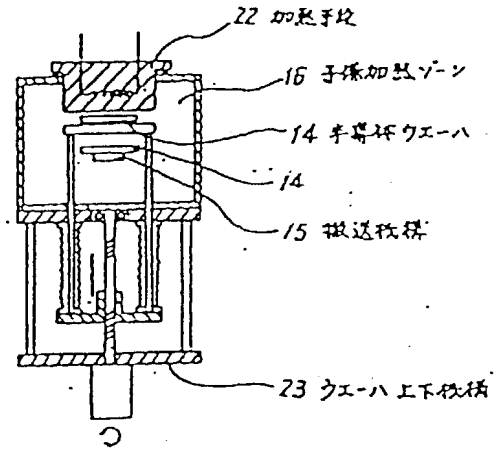

Figure 4

Key: 14 Semiconductor wafer
15 Transport mechanism
16 Preheating zone
22 Heating means
23 Wafer-raising and lowering mechanism

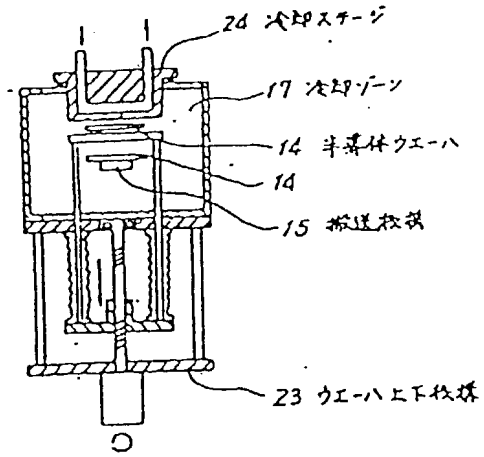

Figure 5

Key: 14 Semiconductor wafer
15 Transport mechanism
17 Cooling zone
23 Wafer-raising and lowering mechanism
24 Cooling stage

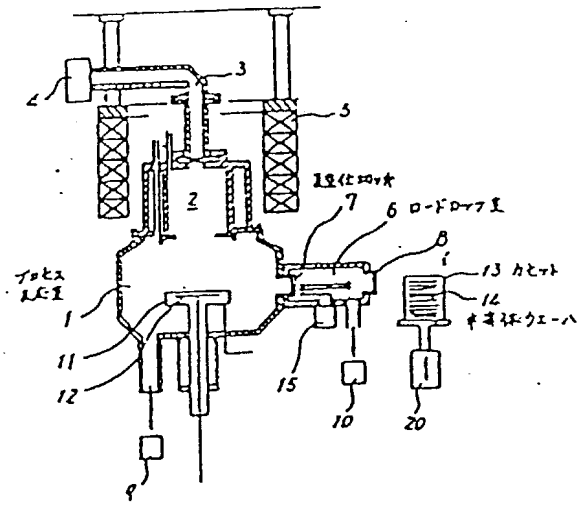

Figure 6

Key: 1 Processor reaction chamber
6 Load-and-lock chamber
7 Vacuum gate valve
13 Cassette
14 Semiconductor wafer

SEMICONDUCTOR WAFER PROCESSOR

SEMICONDUCTOR WAFER PROCESSOR

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Inventor(s):	YOSHIDA MAKOTO
Applicant(s):	FUJI ELECTRIC CO LTD
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EC Classification:	
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Abstract

PURPOSE:To enable a film in excellent quality and high throughput to be formed by a method wherein a carrier system to deliver a wafer is arranged in open state in a vacuum vessel wherein a cassette chamber containing a cassette loaded with semiconductor wafers is formed to be air-tightly coupled so that the wafer may be pre-heated to be cooled down after surface processing.
CONSTITUTION:A cassette 13 is contained in a cassette chamber 18 to be vacuumized. A vacuum sluice valve 19 is opened, a wafer 14 is taken out of the cassette 13 by a carrier system 15 in a load-lock chamber 26 do as to be delivered to a wafer lifting mechanism 23; after processing in a heating zone 16, the wafer 14 is carried to a process reaction chamber 1 to be delivered to a wafer holding mechanism 11. Any processed wafer 14 is carried to the chamber 26 so as to be cooled down by a cooling down means in a cooling down zone B. After the lifting mechanism 23 in the heating zone 16 is shifted to a specified position, the carrier system 15 receives the wafer 14 from the lifting mechanism 23 in the cooling down zone B so as to contain the wafer 14 in the cassette 13 in the cassette chamber 18. Accordingly, the cooled down wafer 14 can be carried to the cassette 13 during the pre-heating process.

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審査請求　未請求　請求項の数 1　(全7頁)

⑤4発明の名称　半導体ウエーハ処理装置

⑳特　願　平1−275217
㉒出　願　平1(1989)10月23日

⑦2発明者　吉田　誠　神奈川県川崎市川崎区田辺新田1番1号　富士電機株式会社内
⑦1出願人　富士電機株式会社　神奈川県川崎市川崎区田辺新田1番1号
⑦4代理人　弁理士　山口　巖

明細書

1. 発明の名称　半導体ウエーハ処理装置

2. 特許請求の範囲

1) 半導体ウエーハを1枚づつ表面処理する枚葉処理方式の半導体ウエーハ処理装置であって、半導体ウエーハに表面処理が施されるプロセス反応室に真空仕切り弁を介して連設された1つの真空容器内に、表面処理前の半導体ウエーハを予備加熱する加熱手段と、表面処理後の半導体ウエーハを冷却する冷却手段と、半導体ウエーハを保持して前進後退、上昇下降、水平旋回させる機能を持ち該真空容器外部から該容器内へ表面処理前の半導体ウエーハを取り込むとともに前記プロセス反応室内のウエーハステージへ前記加熱手段による予備加熱後の半導体ウエーハを受け渡しする搬送機構とが相互間の仕切りを設けることなく開放状態に配設され、かつ該加熱手段と冷却手段とのそれぞれ下方に、半導体ウエーハが載置されて該半導体ウエーハを上下方向に移動させるウエーハ上下機構を備えるとともに該真空容器が加熱手段の反搬送機構側に半導体ウエーハが装填されたカセットを収容するカセット室を気密に結合可能に形成されていることを特徴とする半導体ウエーハ処理装置。

3. 発明の詳細な説明

〔産業上の利用分野〕

この発明は、半導体ウエーハ(以下単にウエーハとも記す)に対し、プラズマCVDなどによる薄膜形成やエッチング等の表面処理をウエーハ1枚づつ順に行う枚葉処理方式の半導体ウエーハ処理装置に関する。

〔従来の技術〕

この種半導体ウエーハ処理装置の従来の構成例を第6図に示す。図において、1はプロセス反応室、2は導波管3を介してマイクロ波発振器としてのマグネトロン4が接続され、かつ室の周域に励磁コイル5が配備されたプラズマ生成室、6はプロセス反応室1に真空仕切弁7を介して隣設されたロードロック室、8はロードロック室6と室外とを仕切る真空仕切り弁、9，10はそれぞれプ

ロセス反応室1およびロードロック室6に接続した真空排気系、11はプラズマ生成室2に対向してプロセス反応室1内に設置した例えば静電チャック12を装備のウエーハ保持機構、13は複数枚の半導体ウエーハ14を並置収容したカセットである。

かかる構成で、プロセス反応室1，プラズマ生成室2を真空排気しておき、プラズマ生成室2内へ目的に応じたプラズマ生成用原料のキャリアガスを外部から供給した状態でマグネトロン4で発振したマイクロ波を導波管3を通じて送り込み、かつ励磁コイル5を通電して磁場を与えることにより、プラズマ生成室内にＥＣＲプラズマが発生する。

これに先立ち、ウエーハは次記の搬送操作によってプロセス反応室1内に1枚送りこまれてウエーハ保持機構11に受け渡し保持される。すなわち、まず、ロードロック室6内にN_2ガスを外部から図示されない管路を通じて導入し、室内を大気圧に復帰させる。次に真空仕切弁8を開き、搬送機構15が未処理ウエーハを収納したカセット13からウエーハ14を1枚抜き取りロードロック室6内に搬入し旋回後プロセス反応室1方向を向いて待機する。ここでロードロック室6は真空排気系10により再び真空状態に保たれ、ロードロック室6の圧力がプロセス反応室1と同等な真空圧に達したところで、次に真空仕切り弁7を開き前記搬送機構15がウエーハ14をプロセス反応室1内に搬入し、室内のウエーハ保持機構11に受け渡すとともに真空仕切り弁7を再び閉じる。

この状態でプロセス反応室1内へ例えばシランガス等の成膜原料ガスを送り込みながら前述のようにＥＣＲプラズマを生成すると、このプラズマがプロセス反応室1内に押し出されて前記シランガスを活性化し、これにより発生した活性種の作用によりウエーハ14の表面にキャリアガスの種類によって異なるシリコン系の各種薄膜が形成されることになる。

一方、所定のウエーハ処理が終了するとウエハ14は前記搬入操作と逆な順序でウエーハ保持機構11よりカセット13に戻され、続いて次のウエーハの処理操作が行われる。またカセット13内に収容されている全てのウエーハ14に付いて処理が済むと、再びロードロック室6の真空仕切り弁8を開放した上でカセット13を室外に搬出し、代わりに次のカセットを搬入して前記と同様な操作でウエーハ処理を行う。

〔発明が解決しようとする課題〕

ところで、このようなプラズマＣＶＤ装置における未処理ウエハは空気中にさらされており、水分の吸着やその他の不純ガスが吸着されており、そのままプロセス処理を行った場合、ボイド等が発生して成膜の膜質を低下させ、ウエーハの品質，歩留りを悪化させる。またこのようなプラズマＣＶＤ装置等で処理された直後のウエーハは高温（約200℃）であり、一方、通常量産装置等で使用されているカセットの材質にはポリプロピレンが用いられている場合が多く、そのまま直ぐにカセットへ搬出するとカセットが変形する問題があった。この問題を解決するために、本願発明者は、鋳込ヒータ等の加熱手段を内蔵した予備加熱室と、水冷等による冷却ステージを内蔵した冷却室とを装備した半導体ウエーハ処理装置を先に考案した。この考案による半導体ウエーハ処理装置は、予備加熱室を第6図におけるロードロック室6のカセット13側に真空仕切り弁8を介して結合するとともに、冷却室を第6図の紙面に垂直方向にロードロック室6と真空仕切り弁を介して結合したものであるが、半導体ウエーハの予備加熱中は表面処理の終了したウエーハをカセット13内へ搬出することができず、また、予備加熱室，ロードロック室，冷却室相互間のウエーハの受渡しの度ごとに真空仕切り弁を開けなければならず、真空仕切り弁の開閉操作に要するロスタイムのため、かかる装置構成では実用量産規模の装置とした場合、スループットに問題が生じるという問題があった。

この発明の目的は、これらの問題点を解決し、スループットが向上した，膜質の良好な成膜が可能な半導体ウエーハ処理装置を提供することである。

〔課題を解決するための手段〕

上記課題を解決するために、この発明においては、半導体ウエーハを1枚づつ表面処理する枚葉処理方式の半導体ウエーハ処理装置を、半導体ウエーハに表面処理が施されるプロセス反応室に真空仕切り弁を介して連設された1つの真空容器内に、表面処理前の半導体ウエーハを予備加熱する加熱手段と、表面処理後の半導体ウエーハを冷却する冷却手段と、半導体ウエーハを保持して前進後退、上昇下降、水平旋回させる機能を持ち該真空容器外部から該容器内へ表面処理前の半導体ウエーハを取り込むとともに前記プロセス反応室内のウエーハステージへ前記加熱手段による予備加熱後の半導体ウエーハを受け渡しする搬送機構とが相互間の仕切りを設けることなく開放状態に配設され、かつ該加熱手段と冷却手段とのそれぞれ下方に、半導体ウエーハが載置されて該半導体ウエーハを上下方向に移動させるウエーハ上下機構を備えるとともに該真空容器が加熱手段の反搬送機構側に半導体ウエーハが装填されたカセットを収容するカセット室を気密に結合可能に形成されている装置とするものとする。

〔作用〕

まず、作用の理解を容易にするために、前記手段に従って構成される半導体ウエーハ処理装置の操作手順につき説明する。

まず、真空仕切り弁を介してロードロック室を構成する真空容器の大気側に結合されたカセット室内を大気圧に復帰しカセットを収納する。収納後真空引きを行う。ロードロック室と連結された真空仕切り弁を開放した状態でロードロック室内の搬送機構によりカセットから1枚ウエーハを取り出し、ロードロック室内に設定され加熱手段が配される加熱ゾーンにおいて該加熱手段の下方に配置されたウエーハ上下機構に受け渡す。次にウエーハ上下機構は加熱ゾーンの最適加熱位置まで移動し加熱処理を行う。処理終了後、ウエーハ上下機構は受渡し位置まで下降し前記搬送機構がウエーハを受取る。ウエーハを受け取った搬送機構は旋回しプロセス反応室を向いて待機する。次いでプロセス反応室と連結された真空仕切り弁が開かれ待機しているウエーハをプロセス反応室内に搬入した上で室内に装備されたウエーハ保持機構に受け渡す。ここで搬送機構をロードロック室内に戻して再び真空仕切り弁を閉じた後にプロセス反応室内で所定のウエーハ処理を行う。ウエーハ処理中に搬送機構は再びカセット室からウエーハを1枚抜き取り加熱ゾーンのウエーハ上下機構に受け渡す。次にウエーハ上下機構は加熱ゾーンの最適位置まで移動し、ウエーハを予備加熱して待機している。

ウエーハ処理が済むと前記した搬入操作と逆な順序で処理済みウエーハがプロセス反応室からロードロック室へ搬出され、前記搬送機構がロードロック室内に設定された冷却ゾーン内の冷却手段下方に配置されたウエーハ上下機構に受け渡す。次にウエーハ上下機構は冷却ゾーンの最適位置へ移動し冷却する。さらに搬送機構は加熱ゾーンのウエーハ上下機構からウエーハを受け取り、前記と同様にプロセス反応室内のウエーハ保持機構に受け渡す。ここで再び所定のウエーハ処理が行われる。次に搬送機構は再びカセット室からウエーハを1枚抜き取り加熱ゾーンのウエーハ上下機構に受け渡す。ここでウエーハ上下機構は加熱ゾーンの最適位置まで移動し、ウエーハを予備加熱して待機している。

加熱ゾーンのウエーハ上下機構が所定の位置へ移動終了後搬送機構は冷却ゾーンのウエーハ上下機構からウエーハを受け取り、加熱ゾーンのウエーハ上下機構の下を通り、カセット室内のカセットの取り出した位置と同じ位置へ収納する。

同様にして設定枚数分の処理が繰り返される。

このように、本発明の装置構成によれば、ウエーハ搬送工程では、カセット室、ロードロック室、プロセス反応室が常に真空に保持されていて大気側に開放されることがなく、水分の吸着、不純ガスの吸着、および外部からの塵埃の侵入が殆どなく室内が高清浄な状態に維持される。これによりプロセス反応室内との間でウエーハを受け渡しする過程でもプロセス反応室内に外部から塵埃等の異物が持ち込まれることが殆どなくなり、かつ予

備加熱によりウエーハ上の水分が除去され、ウエーハに形成される薄膜の質を大幅に向上させることができる。またウエーハ搬送工程でロスタイム発生の要因となる各室間の真空仕切り弁の開閉動作が最少限で済み、かつ全室が常に真空状態であるため、大気圧への復帰および再真空排気といった動作が不要であり、ロスタイムが少なくなるとともに予備加熱中に冷却処理終了のウエーハをカセットへ搬出するといった並列処理が可能となり、一連のウエーハ搬送工程の所要時間を大幅に短縮してスループットの向上を図ることができる。

〔実施例〕

第1図は本発明による半導体ウエーハ処理装置構成の一実施例を示す平面図、第2図は第1図におけるA－A線に沿う装置の縦断面図、第3図は第1図におけるA－B線に沿う装置の縦断面図である。また第4図，第5図はそれぞれ第2図，第3図におけるC－C線，D－D線に沿う断面図であり、第6図に対応する同一部材には同じ符号が付してある。

まず第1図において、プロセス反応室1の側方には真空仕切り弁7を介してロードロック室26が連設配備され、ロードロック室26内には、搬送機構15と加熱ゾーン16と冷却ゾーン17とが配設されている。さらにカセット室18が真空仕切り弁19を介してロードロック室26に連設結合されており、かつ室外大気側とは真空仕切り弁8により仕切られている。そして第2図に示すように、前記カセット室18にはカセット13の段ごとに1ピッチ送りをする送り機構20と真空排気系21とが設けられており、ロードロック室26は鋳込みヒータとして形成された加熱手段22とウエーハ上下機構23とを備える一方、第3図に示すように、ロードロック室26内に水冷による冷却ステージ24とウエーハ上下機構23とが配備されている。

次に上記構成による半導体ウエーハ処理装置におけるウエーハの搬送，処理操作について順を追って説明する。

まず、カセット室18（第2図）を大気圧に復帰しカセット13を収納する。収納後真空排気系21により真空引きを行う。次に真空仕切り弁19を開き搬送機構15がカセット室18内のカセット13からウエーハ14を1枚抜き取りウエーハ上下機構23に受け渡す。ウエーハ上下機構23は、加熱手段22との最適位置までウエーハ14を上昇，近接させ、ここで加熱手段22により予備加熱が行われる。予備加熱処理終了後ウエーハ上下機構23が下降し、再度搬送機構15へウエーハ14が受け渡され、次いで搬送機構15は旋回し、プロセス反応室1を向いて待機し、真空仕切り弁7が開かれると進入し、プロセス反応室1内に装備されたウエーハ保持機構11にウエーハ14を受け渡し、後退後、前記真空仕切り弁7が閉じる。ここで所定のウエーハ処理が行われる。

一方、ウエーハ処理中に、搬送機構15は再びカセット13から前記と同様の手順でウエーハ14を1枚抜き取り、前記予備加熱ゾーン16のウエーハ上下機構23にウエーハを受け渡す。ここでウエーハの予備加熱が行われる。ウエーハを受け渡した搬送機構15はプロセス反応室1を向いた状態で待機している。ウエーハ処理が終了すると前記した搬入操作と逆な順序で搬送機構15が処理済みウエーハ14を搬出する。搬出されたウエーハ14は前記搬送機構15により冷却ゾーン17（第1図，第3図）へ運ばれ、ウエーハ上下機構23へ受け渡される。ここで冷却ステージ24によってウエーハ14は冷却される。一方、冷却ゾーン17へウエーハ14を受け渡した搬送機構15は、加熱ゾーン16で予備加熱されたウエーハ14をプロセス反応室1内のウエーハ保持機構11へ前記と同様な順序で送り込む。ここで再び所定のウエーハ処理が行われる。次に搬送機構15は再びカセット13から前記と同様の手順でウエーハ14を1枚抜き取り、前記予備加熱ゾーン16のウエーハ上下機構23にウエーハを受け渡す。ここで予備加熱が行われる。

次いで搬送機構15は、冷却ゾーン17のウエーハ上下機構23から冷却処理されたウエーハ14を受け取り、カセット13の取り出した位置と同じ位置へ、加熱ゾーン16のウエーハ上下機構23のウエーハ台の下を通過して搬出，挿入する。

以後同様にして設定枚数分の処理が繰り返される。

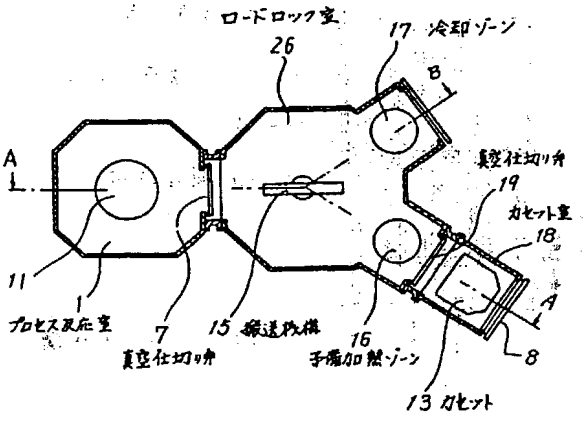
〔発明の効果〕

以上に述べたように、この発明においては、半導体ウエーハを1枚づつ表面処理する枚葉処理方式の半導体ウエーハ処理装置を、半導体ウエーハに表面処理が施されるプロセス反応室に真空仕切り弁を介して連設された1つの真空容器内に、表面処理前の半導体ウエーハを予備加熱する加熱手段と，表面処理後の半導体ウエーハを冷却する冷却手段と，半導体ウエーハを保持して前進後退，上昇下降，水平旋回させる機能を持ち該真空容器外部から該容器内へ表面処理前の半導体ウエーハを取り込むとともに前記プロセス反応室内のウエーハステージへ前記加熱手段による予備加熱後の半導体ウエーハを受け渡しする搬送機構とが相互間の仕切りを設けることなく開放状態に配設され、かつ該加熱手段と冷却手段とのそれぞれ下方に、半導体ウエーハが載置されて該半導体ウエーハを上下方向に移動させるウエーハ上下機構を備えるとともに該真空容器が加熱手段の反搬送機構側に半導体ウエーハが装填されたカセットを収容するカセット室を気密に結合可能に形成されている装置としたので、ウエーハ搬送工程では、カセット室，ロードロック室，プロセス反応室が常に真空に保持されていて大気側に開放されることがなく、水分の吸着，不純ガスの吸着，および外部からの塵埃の侵入が殆どなく室内が高清浄な状態に維持される。これによりプロセス反応室内との間でウエーハを受け渡しする過程でもプロセス反応室内に外部から塵埃等の異物が持ち込まれることが殆どなくなる。また、加熱手段による予備加熱によりウエーハに吸着された水分が除去された状態で表面処理が行われるため、ウエーハに形成される薄膜の膜質が向上し、かつ、この膜質を、最小限の真空仕切り弁の開閉動作と、加熱手段，冷却手段のそれぞれ下方に配されたウエーハ上下機構により可能となる，未処理ウエーハ予備加熱中に冷却終了のウエーハをカセットへ搬出する並列処理とにより、一連のウエーハ搬送工程の所要時間を従来装置と比べ大幅に短縮して得ることができ、スループットが向上する効果が得られる。

4. 図面の簡単な説明

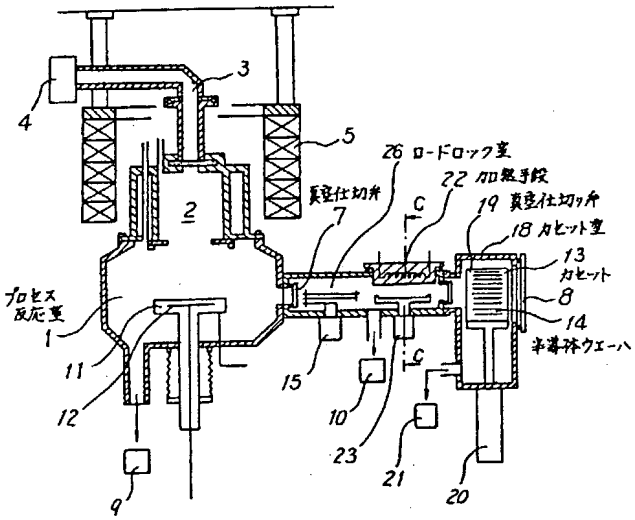
第1図ないし第5図は本発明の一実施例による半導体ウエーハ処理装置の構成を示し、第1図は要部の横断面図、第2図は第1図におけるA－A線に沿う装置の縦断面図、第3図は第1図におけるA－B線に沿う装置の縦断面図、第4図は第2図におけるC－C線に沿う正面断面図、第5図は第3図におけるD－D線に沿う正面断面図、第6図は従来の半導体ウエーハ処理装置の構成例を示す縦断面図である。

1…プロセス反応室、6，26…ロードロック室（真空容器）、7，19…真空仕切り弁、13…カセット、14…半導体ウエーハ、15…搬送機構、16…予備加熱ゾーン、17…冷却ゾーン、18…カセット室、22…加熱手段、23…ウエーハ上下機構、24…冷却ステージ（冷却手段）。

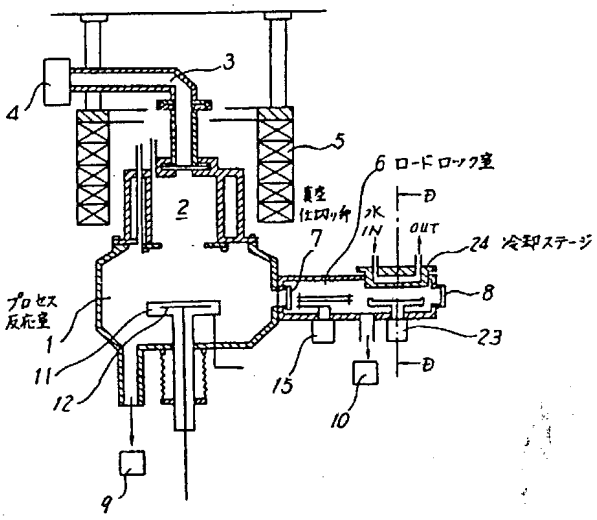


第 1 図

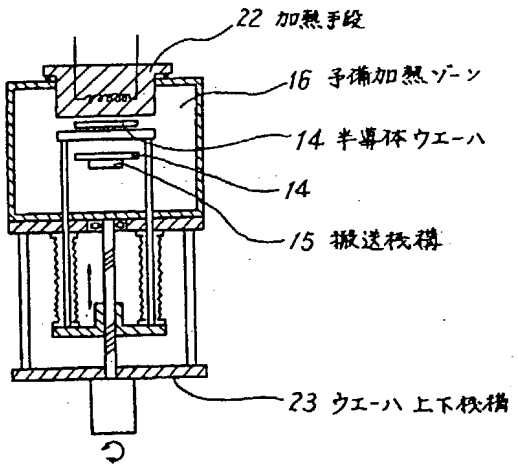
代理人弁理士 山 口 巖



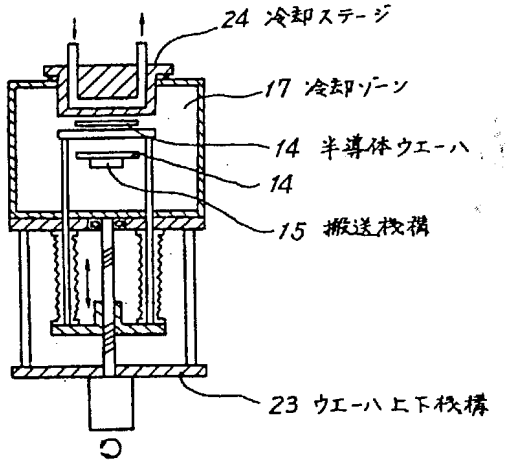
第 2 図



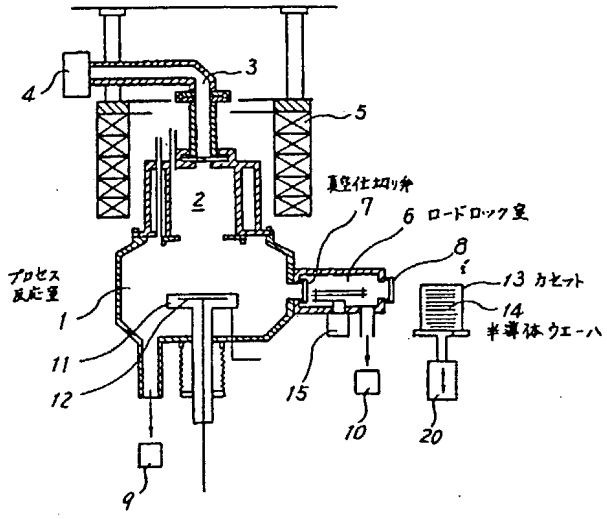
第 3 図



第 4 図



第 5 図


4
3
5
2
真空仕切り弁
7
6 ロードロック室
8
13 カセット
14
半導体ウエーハ
プロセス
反応室
1
11
12
15
10
20
9

第 6 図